Ultralow Distortion, Low Power, Low Noise, High Speed Op Amp

Preliminary Technical Data

ADA4857-1/ADA4857-2

FEATURES

High speed
- **850 MHz, −3 dB bandwidth (G = +1, R_L = 1 kΩ)**
- **2800 V/µs slew rate**

Low distortion: −91 dBc @ 10 MHz (G = +1, R_L = 1 kΩ)
Low power: 5 mA/amplifier @ 10 V
Low noise: 4.4 nV/√Hz
Wide supply voltage range: 5 V to 10 V
Power-down feature
Available in 3 mm × 3 mm 8-lead LFCSP (single), 8-lead SOIC (single), and 4 mm × 4 mm 16-lead LFCSP (dual)

APPLICATIONS

Instrumentation
IF and baseband amplifiers
Active filters
ADC drivers
DAC buffers

CONNECTION DIAGRAM

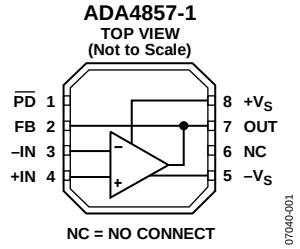

Figure 1. 8-Lead LFCSP (CP)

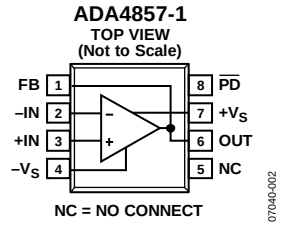

Figure 2. 8-Lead SOIC (R)

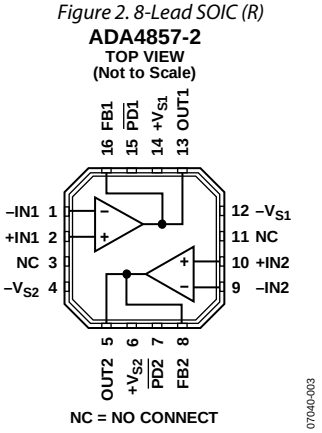

Figure 3. 16-Lead LFCSP (CP)

GENERAL DESCRIPTION

The ADA4857 is a unity gain stable, high speed, voltage feedback amplifier with low distortion, low noise, and high slew rate. With a spurious-free dynamic range of −91 dBc @ 10 MHz, the ADA4857 is an ideal solution in a variety of applications, including ultrasound, ATE, active filters, and ADC drivers. The Analog Devices, Inc. proprietary next-generation XFCB process and innovative amplifier architecture enable such high performance.

The ADA4857 features a low distortion pinout for the LFCSP, which improves second harmonic distortion and simplifies the layout of the circuit board.

The ADA4857 has 850 MHz bandwidth, 2800 V/µs slew rate, and settles to 0.1% in 5 ns. With a wide supply voltage range (5 V to 10 V), the ADA4857 is an ideal candidate for systems that require high dynamic range, precision, and speed.

The ADA4857-1 amplifier is available in a 3 mm × 3 mm, 8-Lead LFCSP and a standard 8-lead SOIC (R-8). The ADA4857-2 is available in a 4 mm × 4 mm, 16-Lead LFSCP. The LFCSP features an exposed paddle that provides a low thermal resistance path to the PCB, which enables more efficient heat transfer and increases reliability. The ADA4857-1 operates over the temperature range of −40°C to +125°C, and the ADA4857-2 operates over the temperature range of −40°C to +105°C.

Rev. PrA

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

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REVISION HISTORY

1/08—Revision 0: Initial Version

SPECIFICATIONS

±5 V SUPPLY

T_A = 25°C, G = +2, R_L = 1 kΩ R_G = R_F = 499 Ω to ground, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_{OUT} = 0.2 V p-p	650	850		MHz
	G = +1, V_{OUT} = 2 V p-p		760		MHz
	G = +2, V_{OUT} = 0.2 V p-p	300	400		MHz
Full Power Bandwidth	G = +1, V_{OUT} = 2 V p-p, THD < −40 dBc		110		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_{OUT} = 2 V p-p, R_L = 150 Ω		100		MHz
Slew Rate	G = +1, V_{OUT} = 6 V step		2800		V/µs
Settling Time to 0.1%	G = +2, V_{OUT} = 2 V step		5		ns
NOISE/HARMONIC PERFORMANCE					
Harmonic Distortion, HD2/HD3 (dBc)	f_C = 1 MHz, V_{OUT} = 2 V p-p		−108		dBc
	f_C = 10 MHz, V_{OUT} = 2 V p-p		−91		dBc
	f_C = 50 MHz, V_{OUT} = 2 V p-p		−57		dBc
Input Voltage Noise	f = 100 kHz		4.4		nV/√Hz
Input Current Noise	f = 100 kHz				pA/√Hz
DC PERFORMANCE					
Input Offset Voltage			0.25	1.0	mV
Input Offset Voltage Drift			1.5	5.7	µV/°C
Input Bias Current			1	1.65	µA
Input Bias Current Drift			5	8.1	nA/°C
Input Bias Offset Current					µA
Open-Loop Gain	V_{OUT} = −3 V to +3 V		60		dB
$\overline{PD}$ Pin					
Disable Input Voltage	Output Disable				V
Turn-Off Time	50% off Disable to <10%				ns
Turn-On Time	50% off Disable to <10%				ns
Enable Pin Leakage Current	Enable = 0 V				µA
Disable Pin Leakage Current	Disable = 5 V				µA
INPUT CHARACTERISTICS					
Input Resistance	Common-mode/differential				MΩ
Input Capacitance	Common-mode				pF
Input Common-Mode Voltage Range			±4		V
Common-Mode Rejection	V_{CM} = ±1 V		−90		dB
OUTPUT CHARACTERISTICS					
Output Overdrive Recovery Time	V_{IN} = ±5 V, G = +1		10		ns
Output Voltage Swing	R_L = 1 kΩ		−4.1 to +4.1		V
	R_L = 100 Ω		−3.75 to +3.75		V
Output Current			50		mA
Short-Circuit Current	Sinking/sourcing				mA
Capacitive Load Drive	30% overshoot, G = +2		~10		pF
POWER SUPPLY					
Operating Range			3.3 – 10		V
Quiescent Current			5		µA
Quiescent Current (Disabled)					µA
Positive Power Supply Rejection	$+V_S$ = +5 V to +6 V, $-V_S$ = −5 V		−64		dB
Negative Power Supply Rejection	$+V_S$ = +5 V, $-V_S$ = −5 V to −6 V		−67		dB

+5 V SUPPLY

T_A = 25°C, G = +2, R_F = R_G = 499 Ω, R_L = 1 kΩ to midsupply, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_{OUT} = 0.2 V p-p	595	770		MHz
	G = +1, V_{OUT} = 2 V p-p		500		MHz
	G = +2, V_{OUT} = 0.2 V p-p	260	360		MHz
Full Power Bandwidth	G = +1, V_{OUT} = 2 V p-p, THD < −40 dBc		95		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_{OUT} = 2 V p-p, R_L = 150 Ω		78		MHz
Slew Rate	G = +1, V_{OUT} = 2 V step		1350		V/µs
Settling Time to 0.1%	G = +2, V_{OUT} = 2 V step		6		ns
NOISE/HARMONIC PERFORMANCE					
Harmonic Distortion, HD2/HD3 (dBc)	f_C = 1 MHz, V_{OUT} = 2 V p-p		−90		dBc
	f_C = 10 MHz, V_{OUT} = 2 V p-p		−70		dBc
	f_C = 50 MHz, V_{OUT} = 2 V p-p		−50		dBc
Input Voltage Noise	f = 100 kHz		4.4		nV/√Hz
Input Current Noise	f = 100 kHz				pA/√Hz
DC PERFORMANCE					
Input Offset Voltage			0.75	1.8	mV
Input Offset Voltage Drift			4.2	7.9	µV/°C
Input Bias Current			1	1.7	µA
Input Bias Current Drift			5	7.5	nA/°C
Input Bias Offset Current					µA
Open-Loop Gain			60		dB
$\overline{PD}$ Pin					
Disable Input Voltage	Output Disable				V
Turn-Off Time	50% off Disable to <10%				ns
Turn-On Time	50% off Disable to <10%				ns
Enable Pin Leakage Current	Enable = 0 V				µA
Disable Pin Leakage Current	Disable = 5 V				µA
INPUT CHARACTERISTICS					
Input Resistance	Common-mode/differential				MΩ
Input Capacitance	Common-mode				pF
Input Common-Mode Voltage Range			±1.5		V
Common-Mode Rejection	V_{CM} = 2 V to 3 V		−88		dB
OUTPUT CHARACTERISTICS					
Overdrive Recovery Time	V_{IN} = −0 V to +5 V, G = +1		10		ns
Output Voltage Swing	R_L = 1 kΩ		−1.7 to +1.7		V
	R_L = 100 Ω		−1.5 to +1.5		V
Output Current			50		mA
Short-Circuit Current	Sinking/sourcing				mA
Capacitive Load Drive	30% overshoot, G = +2		~10		pF
POWER SUPPLY					
Operating Range			3.3 – 10		V
Quiescent Current			5		µA
Quiescent Current (Disabled)					µA
Positive Power Supply Rejection	$+V_S$ = +5 V to +6 V, $-V_S$ = 0 V		−62		dB
Negative Power Supply Rejection	$+V_S$ = +5 V, $-V_S$ = 0 V to −1 V		−67		dB

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	10.6 V
Power Dissipation	See Figure 4
Common-Mode Input Voltage	$-V_S - 0.7$ V to $+V_S + 0.7$ V
Differential Input Voltage	$\pm V_S$
Exposed Paddle Voltage	$-V_S$
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +105°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, θ_{JA} is specified for device soldered in circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC	115	15	°C/W
8-Lead LFCSP	94.5	34.8	°C/W
16-Lead LFSCP	68.2	19	°C/W

Maximum Power Dissipation

The maximum safe power dissipation for the ADA4857 is limited by the associated rise in junction temperature (T_J) on the die. At approximately 150°C, which is the glass transition temperature, the properties of the plastic change. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADA4857. Exceeding a junction temperature of 175°C for an extended period can result in changes in silicon devices, potentially causing degradation or loss of functionality.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the die due to the ADA4857 drive at the output. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S).

$$P_D = \textit{Quiescent Power} + (\textit{Total Drive Power} - \textit{Load Power})$$

$$P_D = (V_S \times I_S) + \left(\frac{V_S}{2} \times \frac{V_{OUT}}{R_L}\right) - \frac{{V_{OUT}}^2}{R_L}$$

RMS output voltages should be considered. If R_L is referenced to $-V_S$, as in single-supply operation, the total drive power is $V_S \times I_{OUT}$. If the rms signal levels are indeterminate, consider the worst case, when $V_{OUT} = V_S/4$ for R_L to midsupply.

$$P_D = (V_S \times I_S) + \frac{(V_S/4)^2}{R_L}$$

In single-supply operation with R_L referenced to $-V_S$, worst case is $V_{OUT} = V_S/2$.

Airflow increases heat dissipation, effectively reducing θ_{JA}. Also, more metal directly in contact with the package leads and exposed paddle from metal traces, through holes, ground, and power planes reduce θ_{JA}.

Figure 4 shows the maximum safe power dissipation in the package versus the ambient temperature for the SOIC and LFCSP packages on a JEDEC standard 4-layer board. θ_{JA} values are approximations.

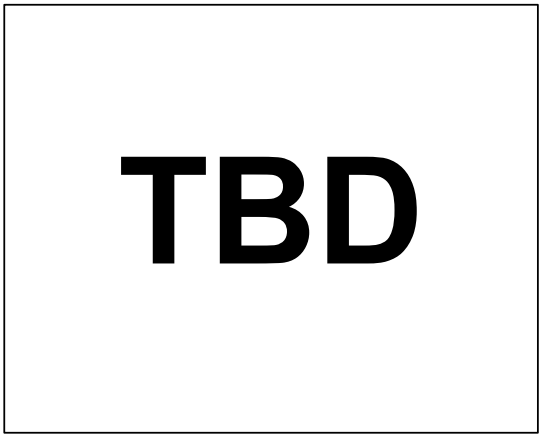

Figure 4. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

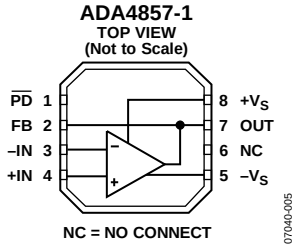

Figure 5. 8-Lead LFCSP Pin Configuration

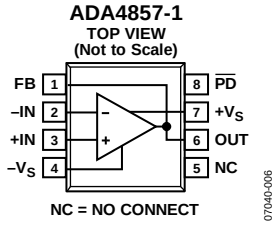

Figure 6. 8-Lead SOIC Pin Configuration

Table 5. 8-Lead LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{PD}$	Power Down.
2	FB	Feedback Pin.
3	−IN	Inverting Input.
4	+IN	Noninverting Input.
5	$-V_S$	Negative Supply.
6	NC	No Connect.
7	OUT	Output.
8	$+V_S$	Positive Supply.

Table 6. 8-Lead SOIC Pin Function Descriptions

Pin No.	Mnemonic	Description
1	FB	Feedback Pin.
2	−IN	Inverting Input.
3	+IN	Noninverting Input.
4	$-V_S$	Negative Supply.
5	NC	No Connect.
6	OUT	Output.
7	$+V_S$	Positive Supply.
8	$\overline{PD}$	Power Down.

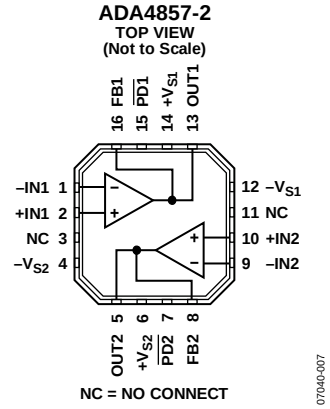

Figure 7. 16-Lead LFCSP Pin Configuration

Table 7. 16-Lead LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	−IN1	Inverting Input 1.
2	+IN1	Noninverting Input 1.
3, 11	NC	No Connect.
4	$-V_{S2}$	Negative Supply 2.
5	OUT2	Output 2.
6	$+V_{S2}$	Positive Supply 2.
7	$\overline{PD2}$	Power Down 2.
8	FB2	Feedback Pin 2.
9	−IN2	Inverting Input 2.
10	+IN2	Noninverting Input 2.
12	$-V_{S1}$	Negative Supply 1.
13	OUT1	Output 1.
14	$+V_{S1}$	Positive Supply 1.
15	$\overline{PD1}$	Power Down 1.
16	FB1	Feedback Pin 1.

APPLICATIONS INFORMATION

RECOMMENDED VALUES FOR VARIOUS GAINS

Table 8 provides a handy reference for determining various gains and associated performance. Resistors R_F and R_G are kept low to minimize their contribution to the overall noise performance of the amplifier.

Table 8. Conditions: V_S = ±5 V, T_A = 25°C, R_L = 1 kΩ

Gain	R_F (Ω)	R_G (Ω)	−3 dB SS BW (MHz) (25 mV p-p)	Slew Rate (V/µs) (2 V Step)	ADA4857 Output Noise (nV/√Hz)	Total Output Noise (nV/√Hz)
+1	0	NA	605	274	1	1.2
−1	100	100	294	265	2	2.7
+2	100	100	277	253	2	2.7
+5	200	49.9	77	227	5	6.5
+10	453	49.9	37	161	10	13.3

$\overline{PD}$ PIN OPERATION

The $\overline{PD}$ pin is used to disable the chip, which reduces the quiescent current and the over all power consumption.

CIRCUIT CONSIDERATIONS

Careful and deliberate attention to detail when laying out the ADA4857 board yields optimal performance. Power supply bypassing, parasitic capacitance, and component selection all contribute to the overall performance of the amplifier.

GROUNDING

Ground and power planes should be used where possible. Ground and power planes reduce the resistance and inductance of the power planes and ground returns. The returns for the input, output terminations, bypass capacitors, and R_G should all be kept as close to the ADA4857 as possible. The output load ground and the bypass capacitor grounds should be returned to the same point on the ground plane to minimize parasitic trace inductance, ringing, and overshoot and to improve distortion performance.

The ADA4857 LFSCP packages feature an exposed paddle. For optimum electrical and thermal performance, solder this paddle to ground. For more information on high speed circuit design, see *A Practical Guide to High-Speed Printed-Circuit-Board Layout*.

OUTLINE DIMENSIONS

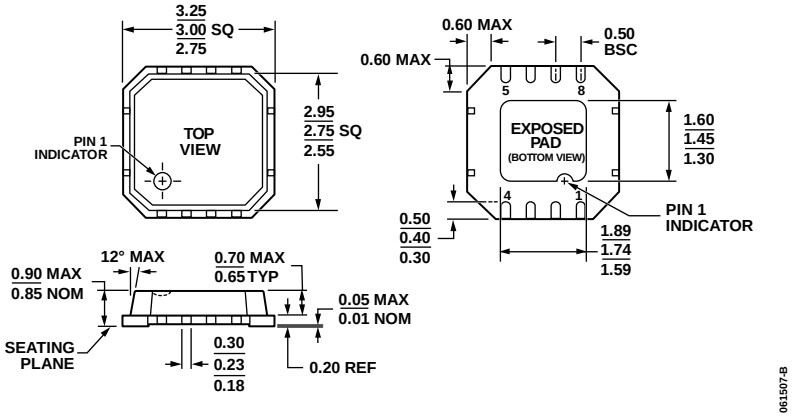

Figure 8. 8-Lead Lead Frame Chip Scale Package [LFCSP_VD]
3 mm × 3 mm Body, Very Thin, Dual Lead (CP-8-2)
Dimensions shown in millimeters

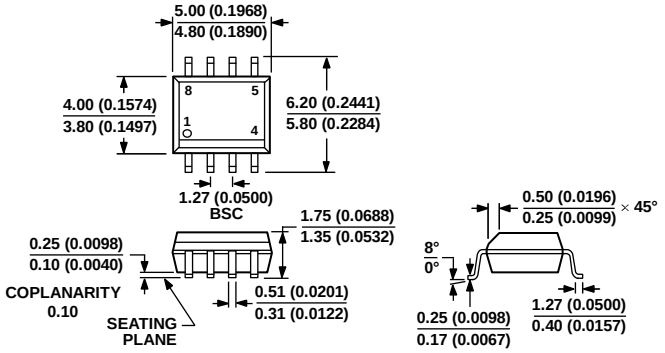

Figure 9. 8-Lead Standard Small Outline Package [SOIC_N]
(R-8)
Dimensions shown in millimeters and (inches)

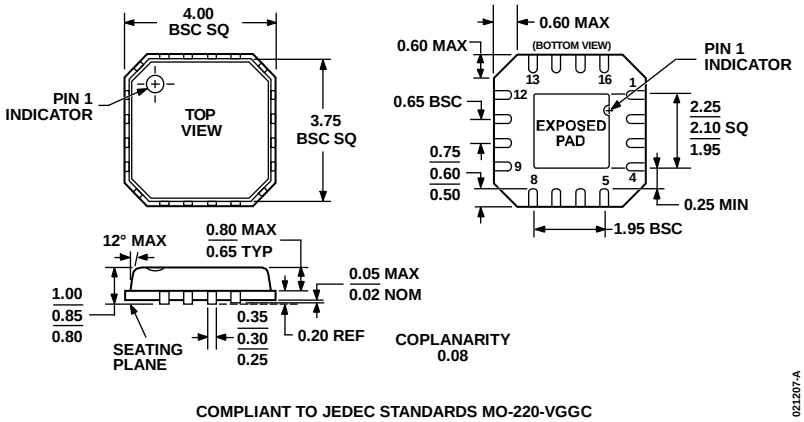

Figure 10. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-16-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Ordering Quantity	Temperature Range	Package Description	Package Option	Branding
ADA4857-1YCPZ-R2[1]	250	–40°C to +125°C	8-Lead LFCSP_VD	CP-8-2	H15
ADA4857-1YCPZ-RL[1]	5,000	–40°C to +125°C	8-Lead LFCSP_VD	CP-8-2	H15
ADA4857-1YCPZ-R7[1]	1,500	–40°C to +125°C	8-Lead LFCSP_VD	CP-8-2	H15
ADA4857-1YRZ[1]	250	–40°C to +125°C	8-lead SOIC_N	R-8	
ADA4857-1YRZ-R7[1]	5,000	–40°C to +125°C	8-lead SOIC_N	R-8	
ADA4857-1YRZ-RL[1]	1,500	–40°C to +125°C	8-lead SOIC_N	R-8	
ADA4857-2YCPZ-R2[1]	250	–40°C to +105°C	16-Lead LFSCP_VQ	CP-16-4	
ADA4857-2YCPZ-RL[1]	5,000	–40°C to +105°C	16-Lead LFSCP_VQ	CP-16-4	
ADA4857-2YCPZ-R7[1]	1,500	–40°C to +105°C	16-Lead LFSCP_VQ	CP-16-4	

[1] Z = RoHS Compliant Part.

NOTES

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